We claim:

1. A method for driving a plasma display panel, wherein a display field, corresponding to a display of a screen, is composed of a plurality of subfields, a gradation display is realized by combining subfields to be lit among the plurality of subfields, each subfield comprises at least an address period to write cells to be lit in the subfield and a sustain period to cause light emission to occur in the written cells, and all of the cells to be lit in a display field are lit in a predetermined subfield among the plurality of subfields making up the display field.

2. A method for driving a plasma display panel, as set forth in claim 1, wherein the predetermined subfield is a subfield with the lowest luminance ratio.

3. A method for driving a plasma display panel, as set forth in claim 1, wherein a display field has a subfield with a same luminance ratio as that of the predetermined subfield, in addition to the predetermined subfield.

4. A method for driving a plasma display panel, as set forth in claim 1, wherein the predetermined subfield is the subfield at the head in a display field.

5. A method for driving a plasma display panel, as set forth in claim 1, wherein an all-cell write discharge is caused to occur in the predetermined subfield before the address period.

6. A method for driving a plasma display panel, as set forth in claim 1, wherein an all-cell write discharge is caused to occur in the predetermined subfield and a subfield with a heavy weight of luminance before the address period.

7. A method for driving a plasma display panel, as set forth in claim 5, wherein the all-cell write discharge is caused to occur twice successively in the predetermined subfield.

8. A method for driving a plasma display panel, as

set forth in claim 5, wherein a subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the subfield immediately before the subfield in which the all-cell write discharge is caused to occur.

9. A method for driving a plasma display panel, as set forth in claim 1, wherein the subfield with the lowest luminance ratio is arranged at the head in a display field and the predetermined subfield is arranged in the second position in the display field.

10. A method for driving a plasma display panel, as set forth in claim 9, wherein the predetermined subfield is one with the second lowest luminance ratio.

11. A method for driving a plasma display panel, as set forth in claim 9, wherein an all-cell write discharge is caused to occur in the subfield at the head and the predetermined subfield before the address period.

12. A method for driving a plasma display panel, as set forth in claim 9, wherein a subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the subfield at the head.

13. A method for driving a plasma display panel, as set forth in claim 1, wherein the widths of an address pulse and a scan pulse during the address period in the predetermined subfield are wider than those of the address pulse and the scan pulse during the address period in other subfields.

14. A method for driving a plasma display panel, as set forth in claim 1, wherein the voltage of an address pulse during the address period in the predetermined subfield is greater than that of the address pulse during the address period in other subfields.

15. A method for driving a plasma display panel, as set forth in claim 1, wherein the voltage of a scan pulse during the address period in the predetermined subfield is greater than that of the scan pulse during the address period in other subfields.

16. A method for driving a plasma display panel, as set forth in claim 1, wherein a process to suppress a discharge in an unlit cell is performed between the address period and the sustain period in the predetermined subfield.

17. A method for driving a plasma display panel, as set forth in claim 16, wherein the process to suppress a discharge in an unlit cell is a process in which, at the same time an address pulse is applied to an address electrode, a pulse, the applied voltage of which varies as time elapses, is applied to a scan electrode.

18. A method for driving a plasma display panel, as set forth in claim 17, wherein the final potential of the pulse, the applied voltage of which varies as time elapses, is lower than the finally reached potential of a charge control pulse, which is applied after an all-cell write discharge and the applied voltage of which varies as time elapses.

19. A method for driving a plasma display panel, as set forth in claim 1, wherein the gradation display level is determined with the luminance due to lighting in the predetermined subfield being taken into consideration.

20. A plasma display device comprising a plasma display panel and a driving circuit for the plasma display panel, wherein the driving circuit drives the plasma display panel using the driving methods set forth in claim 1.